UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,705	12/21/2001	Mauricio Calle	10-6-2	3881

7590 11/08/2005

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
DAVIS, CYNTHIA L	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/029,705	CALLE ET AL.	
	Examiner	Art Unit	
	Cynthia L. Davis	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/14/2005 have been fully considered but they are not persuasive. Regarding claims 1 and 17, a first pass classification and second pass classification being performed on a packet may refer to any steps in the processing of that packet that classifies where that packet is going to be sent. Chong performs various stages of processing on packets; these stages may be viewed as first and second pass classifications.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-6, 9, 1 1-15, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chong.

Regarding claim 1, first classification circuitry, first memory circuitry coupled to the first classification circuitry, the first memory circuitry being configurable to store at least a portion of a given packet to be processed by the first classification circuitry are disclosed in Chong, column 6, lines 17-19 (the receiver circuitry extracts and stores the header information in a memory). Second classification circuitry; and second memory circuitry coupled to the second classification circuitry, the second memory circuitry being

configurable to store at least a portion of the given packet to permit processing thereof by the second classification circuitry is disclosed in Chong, column 6, lines 17-19 (the payload is sent to a different memory) and column 2, lines 5-6. Wherein the first classification circuitry is operative to perform a first pass classification on the given packet, and further wherein the portion of the given packet storable in the second memory circuitry comprises a portion of the given packet determined by the first pass classification to be required for a second pass classification performed by the second classification circuitry is disclosed in Chong, column 6, lines 17-19 (the receiver circuitry determines which part of the cell is the payload and which is the header, and sends the payload for further processing). The first classification circuitry in processing a plurality of packets comprises the given packet and an additional packet generates respective first and second first pass classification determinations that are different from one another and that result in different-size portions of the respective packets being stored in the second memory circuitry for processing by the second classification circuitry is disclosed in Chong, column 6, lines 19-21 (both the extracted header and the VC descriptor address are generated by the first classification; both are stored in the receiver block memory, and both are used for further processing of the packets).

Regarding claim 2, the processor is configured to provide an interface between a network from which the packet is received and a switch fabric is disclosed in column 6, lines 59-64 (disclosing the invention being implemented in a switch in a packet network).

Regarding claim 3, the portion of the given packet storable in the second memory circuitry comprises at least a payload portion of the packet from which at least one of a header and a trailer have been removed is disclosed in column 2, lines 5-6.

Regarding claim 4, the portion of the given packet storable in the second memory circuitry comprises at least a portion of the packet from which information added to the packet in an associated traffic management process has been removed is disclosed in column 6, lines 17-19 (the header has been removed).

Regarding claim 5, the first memory circuitry comprises a first internal memory of the processor coupled to the first classification circuitry via a first memory controller is disclosed in figure 1, element 80, and column 6, lines 17-24 (disclosing storing the VC descriptor formed from the packet header in an internal memory; also header is stored in an internal memory when it is extracted).

Regarding claim 6, the second memory circuitry comprises an internal buffer memory of the processor coupled to the second classification circuitry via a second memory controller is disclosed in column 2, lines 5-6.

Regarding claim 9, the first pass classification is configured to perform at least a portion of a reassembly operation for the given packet, such that a portion of the packet required for performing the reassembly operation need not be stored in the second memory circuitry is disclosed in column 6, lines 10-1 1.

Regarding claim 11, the first pass classification comprises at least one of a reassembly operation, a parity check and a priority determination is disclosed in column 6, lines 10-11.

Regarding claim 12, the first pass classification generates information which is passed in a specified data structure to the second classification circuitry for use in the second pass classification is disclosed in column 6, lines 30-33.

Regarding claim 13, the first pass classification is performed on a plurality of cells comprising the given packet is disclosed in Chong, column 2, lines 3-5.

Regarding claim 14, the portion of the given packet determined by the first pass classification is determined in accordance with one or more instructions provided to the processor under control of a host device operatively coupled to the processor is disclosed in column 6, lines 43-46 (disclosing connection to a host computer system). Regarding claim 15, the processor comprises a network processor is disclosed in Chong, column 2, line 1.

Regarding claim 17, storing in the first memory circuitry at least a portion of a given packet to be processed by the first classification circuitry; and performing in the first classification circuitry a first pass classification on the given packet are disclosed in Chong, column 6, lines 17-19 (the receiver circuitry extracts and stores the header information in a memory). A portion of the given packet storable in the second memory circuitry comprises a portion of the given packet determined by the first pass classification to be required for a second pass classification to be performed by the second classification circuitry is disclosed in Chong, column 6, lines 17-19 (the receiver circuitry determines which part of the cell is the payload and which is the header, and sends the payload for further processing). The first classification circuitry in processing a plurality of packets comprising the given packet and an additional packet generates

respective first and second first pass classification determinations that are different from one another and that result in different sized portions of the respective packets being stored in the second memory circuitry for processing by the second classification circuitry is disclosed in Chong, column 6, lines 19-21 (both the extracted header and the VC descriptor address are generated by the first classification; both are stored in the receiver block memory, and both are used for further processing of the packets).

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Hedley. The first memory circuitry and the second memory circuitry comprise different portions of a single memory internal to the processor is missing from Chong. However, using two parts of a single memory in place of two separate memory entities is disclosed in Hedley, column 8, lines 51-54. It would have been obvious to one skilled in the art at the time of the invention to use two parts of one memory to implement the memories of Chong. The motivation would be to use less hardware to implement the switch.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong. The second memory circuitry has a larger storage capacity than the first memory circuitry is not specifically disclosed in Chong. However, Chong does disclose that the first memory stores the packet header, and the second stores the packet payload, in column 6, lines 17-19 and column 2, lines 5-6. The payload of a packet is larger than

the header. It would have been obvious to one skilled in the art at the time of the invention to make the second memory larger than the first. The motivation would be to have the memories be proportionally sized to the data that is stored in them.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Walker. The first pass classification is configured to perform a parity check for the given packet, such that a portion of the packet required for performing the parity check need not be stored in the second memory circuitry is missing from Chong. However, Walker discloses in column 10, line 66-column 11, line 7, a switch performing a parity check on a received packet. It would have been obvious to one skilled in the art at the time of the invention perform a parity check on the received packet of Chong before storing the payload in the buffer memory. The motivation would be to check for errors in the packet.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chong in view of Erickson. The processor is configured as an integrated circuit is missing from Chong. However, Erickson discloses in column 4, lines 45-49, a switch receiver processor implemented in IC's. It would have been obvious to one skilled in the art at the time pf the invention to use IC's to implement the process of Chong. The motivation would be to use a commercially available type of hardware to implement the processor.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia L. Davis whose telephone number is (571) 272-3117. The examiner can normally be reached on 8:30 to 6, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLD
10/26/2005

CLD
10/26/05

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600